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APPLICATION NOTE

TDA8790M
EVALUATION BOARD DOCUMENTATION

AN/96031

APPLICATION NOTE

TDA8790M
EVALUATION BOARD DOCUMENTATION

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Summary

This note describes a demonstration board which facilitates the evaluation of the TDA8790M 8 bit analog to digital converter.
In addition the operation of the TDA8790M is shortly described and several methods to provide input offset , clamp, and top and bottom references are shown.

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1. INTRODUCTION

The TDA8790M is a 8 bit high speed, low voltage, low power analog to digital converter (30 mW typical at 3.3 V, 4 mW in standby mode).
It has been designed for video signal digitizing, radio communication, camcorders & all applications where size and power saving are strong requirements.
The supplies can be set in the range of 2.7 V up to 5.5V (down to 2.5 V for output supply). The sampling frequency can reach 40 MHz.
Application requires few external components.
TDA8790M comes in a plastic thin quad flat package SSOP20 (SOT266-1), with the following overall body dimensions: 6.5x4.4x1.3 mm^3.

The evaluation board described in this note was designed to allow a quick evaluation of the main TDA8790 characteristics. It is realized with a two layer PCB.

The following features are included :

- One single power supply (+8V +/-10%) is required to generate the supplies needed by the on-board ICs. Connection via banana plugs or grips is possible. To avoid supply connection errors, a green LED is on when the supply polarity is respected. A protection diode is also included to avoid any damage if an error occurs.

- A high-speed 8-bit D/A converter TDA8702T for reconstrucion of the analog signal from the digital data output by TDA8790M. Because this D/A converter is not perfect, its analog output should not be used to characterize the TDA8790M.

- A 40 MHz on-board quartz oscillator or an external clock can be used to control the TDA8790M. Additionally, the clock of the TDA8702T D/A converter can be either the same clock as the one used for TDA8790M (external clock or on board oscillator) or an independent external clock.

- A 7805 regulator generates the 5V supply voltages needed by the D/A converter and the on-board clock oscillator.

- A Texas Instruments TL431 reference supplies the supply voltage (switchable between +3.3V and +5V) and reference voltages for the TDA8790M. It is also possible to input directly the VDD supply voltage of the A/D converter through grip point TM3.

- Selection between on-board generated and external VRT (to be input on grip point TM1) A/D converter top reference voltage.

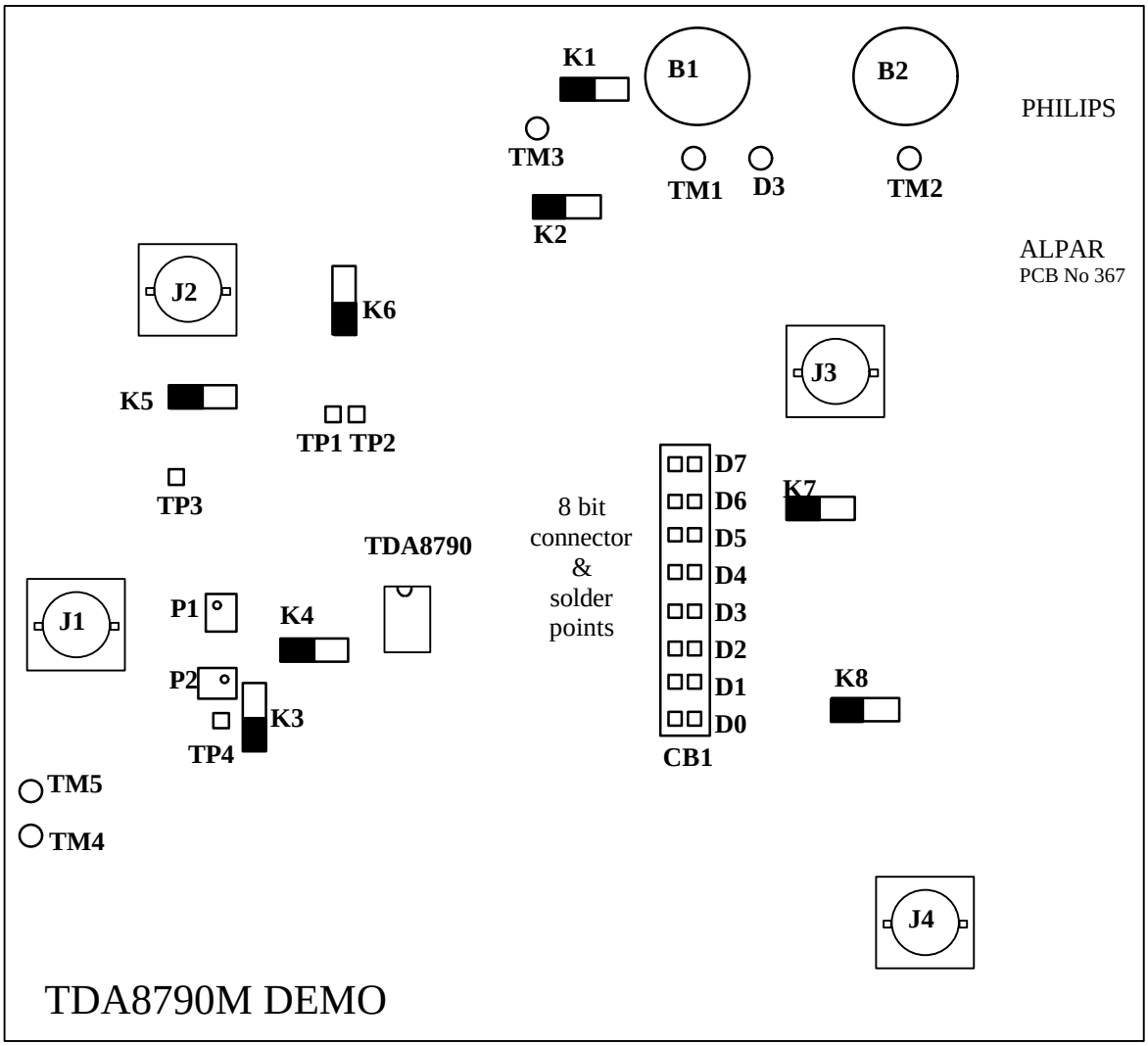
- Probe connectors (CB1 for TDA8790M output bits and test points TP1, TP2 for the A/D converter clock signal and its ground) allow to connect a digital analyzer to the board and to perform digital treatment on the data output by TDA8790M.

- AC input signals only are allowed. The input offset is provided by a resistor bridge.

- All decoupling components necessary for good operation of the TDA8790M are included on board.

2. BOARD DESCRIPTION

2.1 CONNECTORS, POTENTIOMETERS AND SWITCHES POSITIONS

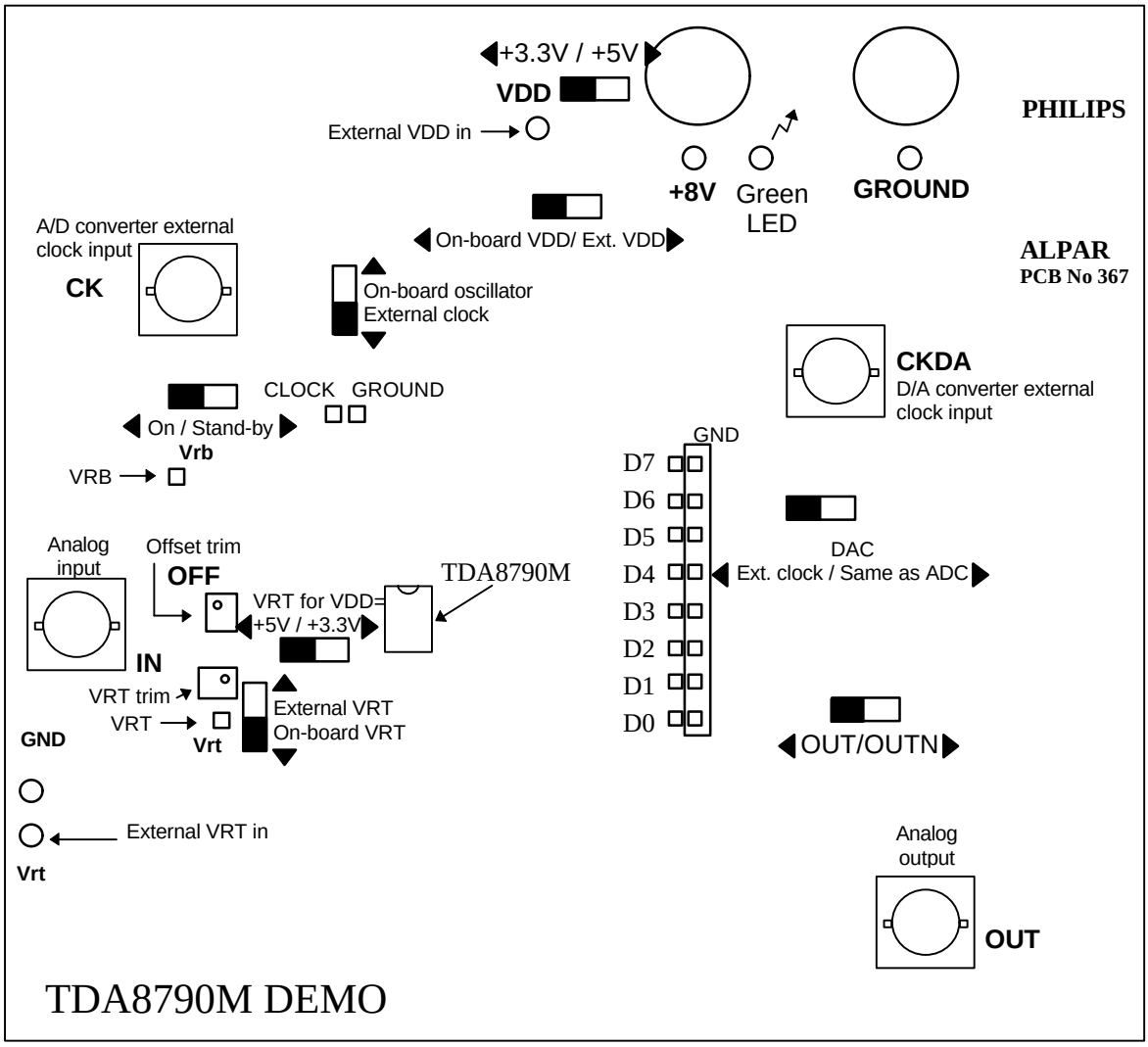


2.2 CONNECTORS, POTENTIOMETERS AND SWITCHES LIST

Reference	Type	Function
B1	Banana PLUG	External board supply (8V)
B2	Banana PLUG	External board supply (ground)
CB1	test point array	TDA8790M output data D7 to D0 with respective grounds.
D3	LED	Green LED, is ON when the power supply is on
J1	BNC	Signal input (50 Ω input)
J2	BNC	ADC (or ADC+DAC) clock input (50 Ω input)
J3	BNC	DAC clock input (50 Ω input)
J4	BNC	DAC output
K1	switch	A/D converter power supply selection (between on-board generated +5V and on-board generated +3.3V).
K2	switch	External/On-board generated A/D converter power supply selction. When external power supply is chosen, the supply voltage must be applied on grip point TM5. The +8V power supply (J13, J14) is still needed for the clock oscillator and D/A converter power supplies generation.
K3	switch	Selection of the A/D converter top reference voltage VRT between external and on-board generated voltages.
K4	switch	A/D converter on-board top reference selection. The two options are : 1) VRT= VDDA (should be used when VDDA=3.3V) 2) VRT derivated from VDDA through potentiometer P3 (when VDDA=5V, default setting in this configuration is VRT=3.3V)
K5	switch	A/D converter Stand-By mode selection.
K6	switch	A/D converter clock selection. The 2 options are : 1) A/D converter clock = on-board generated 40 MHz clock 2) A/D converter clock = external clock

Reference	Type	Function
K7	switch	D/A converter clock selection. The 2 options are : 1) D/A converter clock = A/D converter clock 2) D/A converter clock = external clock
K8	switch	Selection of the D/A converter analog output signal polarity.
P1	potentiometer	2K potentiometer used to set the DC offset of the A/D converter analog input signal
P2	potentiometer	5K potentiometer used to set the A/D converter top reference voltage when this voltage is not set equal to VDDA via switch K24
TM1	grip point	External board supply (+8V)
TM2	grip point	External board supply (ground)
TM3	grip point	External A/D converter supply (2.7 to 5.5 V)
TM4	grip point	External top reference voltage (VRT) input
TM5	grip point	Analog ground (close to TM1)
TP1	test point	A/D converter clock signal.
TP2	test point	A/D converter clock ground.
TP3	test point	A/D converter bottom reference voltage.
TP4	test point	A/D converter top reference voltage.

2.3 CONNECTORS, POTENTIOMETERS AND SWITCHES ROLE



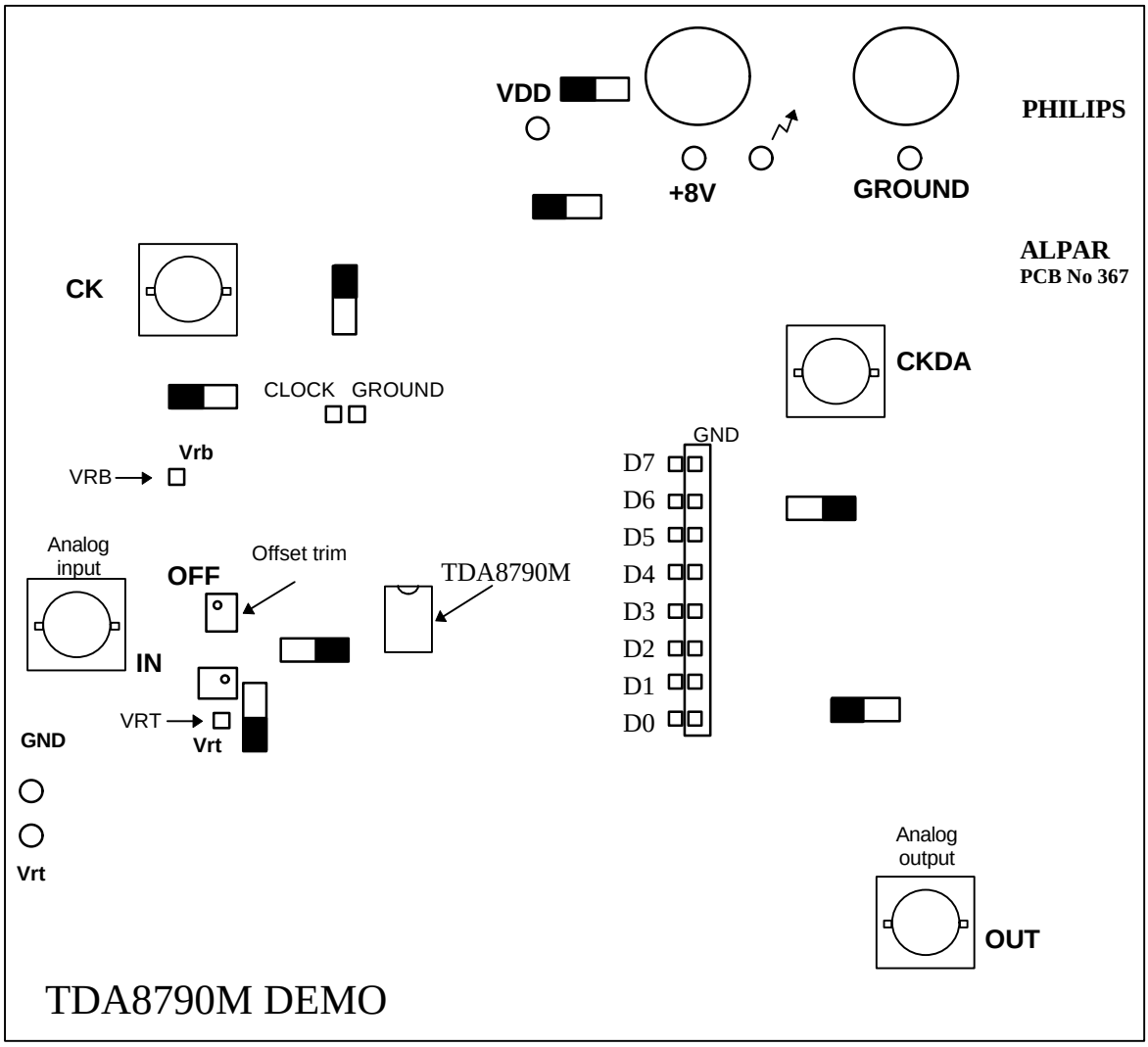
3. EXAMPLES OF BOARD SETTINGS

3.1 INITIAL SETTINGS : 3.3 V ADC SUPPLIES, AC COUPLED INPUT, 40 MHz CLOCK (ON BOARD), 3.3 V and » 1.2 V VOLTAGE REFERENCES

The boards are delivered set in the following configuration :
- On-board generated TDA8790M supply voltage VDD is selected. It is set to +3.3V.
- On-board generated VRT reference voltage is used. It is set to VRT = VDDA (+3.3V in the present case).
- On-board generated + 40 MHz clock signal is used for both A/D converter and D/A converter.
- Potentiometer P1 is adjusted to provide a mid-scale code output when no analog signal is input, in the given supply (VDD) and top reference voltage (VRT) conditions.
- Sleep mode (stand-by mode) is inactive.
- TDA8702T D/A converter output is not inverted.

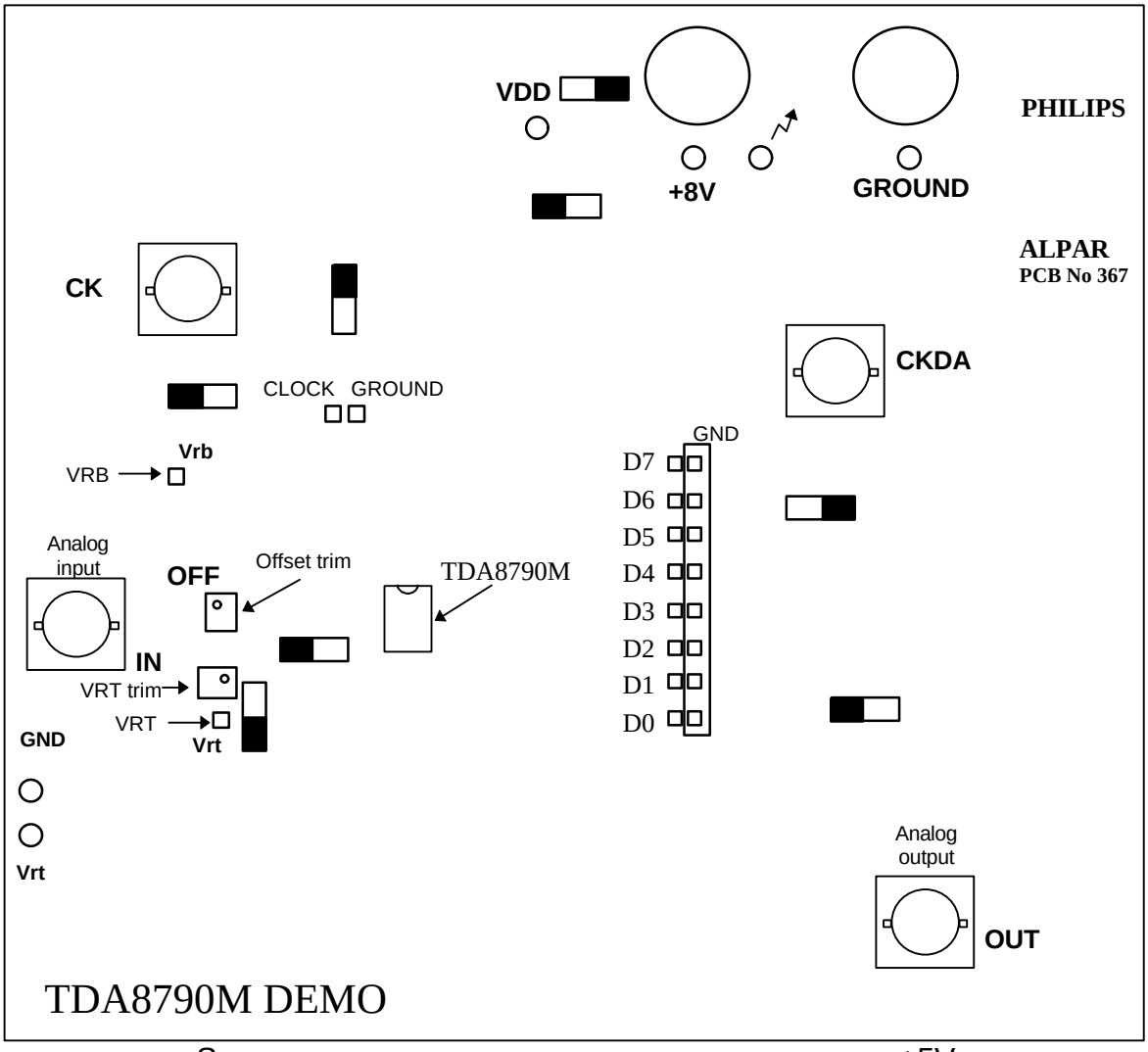
The board supply must be set at 8 V.

In this configuration the analog input signal source must be provided by an external generator which is connected to the board by the J1 connector (dynamic input impedance: 50 Ω).



SWITCHES POSITION FOR ON-BOARD GENERATED VDD=+3.3V
ON-BOARD GENERATED VRT AND CLOCK SIGNALS FOR A/D CONVERTER AND D/A CONVERTER
(40 MHZ CLOCK) ARE USED (INITIAL SETTINGS)

3.2 OTHER SETTINGS EXAMPLE : 5 V ADC SUPPLIES, AC COUPLED INPUT, 40 MHz CLOCK (ON BOARD), 3.3 V and » 1.2 V VOLTAGE REFERENCES



SWITCHES POSITION FOR ON-BOARD GENERATED VDD=+5V

ON-BOARD GENERATED VRT AND CLOCK SIGNALS FOR A/D CONVERTER AND D/A CONVERTER (40 MHZ CLOCK) ARE USED

4. A/D CONVERTER SUPPLIES

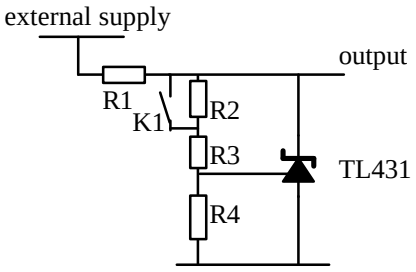
The TDA8790M can work with all supply voltages in the range of 2.7 V to 5.5 V: analog supply (VDDA), digital supply (VDDD), output supply (VDDO). Furthermore, VDDO can be set as low as 2.5 V.
The only restriction for the supplies is to respect the following conditions:

-0.2V < VDDA-VDDD < 0.2V
-0.2V < VDDD-VDDO < 3V
-0.2V < VDDA-VDDO < 3V

4.1 ON-BOARD SUPPLIES GENERATION

The A/D converter supplies (VDDA=VDDD=VDDO) are provided by an adjustable precision regulator (TL431, IC3).

The IC3 regulator output voltages are adjustable by a resistor ratio (see figure).
The formula which gives the regulated voltage related to the resistor ratio is :



Vout = 2.5*(1+(R2+R3)/R4)
or
Vout = 2.5*(1+R3/R4)
depending on K1 position

The power consumption of the TL431 is volontarily set higher than necessary in order to allow different A/D converter voltage supplies.
On board generated A/D converter supplies can be switched between 3.3 V and 5 V via swith K1.

4.2 ON-BOARD / EXTERNAL SUPPLY SELECTION

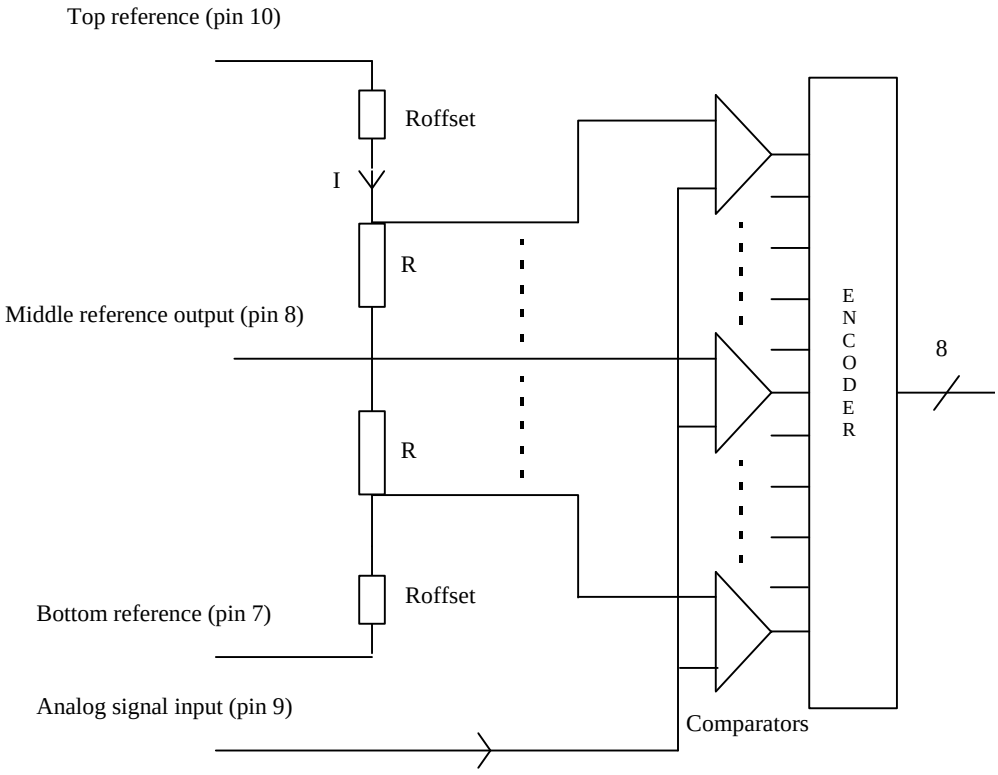
It is also possible to choose between the voltage generated by the TL431 and an externally generated voltage for the TDA8790M A/D converter supply voltages (VDDA=VDDD=VDDO). The choice is made via switch K2. In the case the external supply voltage is chosen, it must be supplied through grip point TM3.

It is also possible to replace resistors R1, R2, R3, R4 with values more suited to one’s peculiar purpose. Be sure to respect the difference limits between the suplies.

In this case, the oscillator and D/A converter supply voltages are still generated by the 7805 regulator (IC4) which must still be supplied by the external +8V supply voltage.

5. VOLTAGE REFERENCES

Here is a block diagram which explains the TDA8790 operation :



During the A to D conversion the analog input signal (pin9) is compared to voltage references by the means of voltage comparators (In fact these comparators are folding amplifiers).

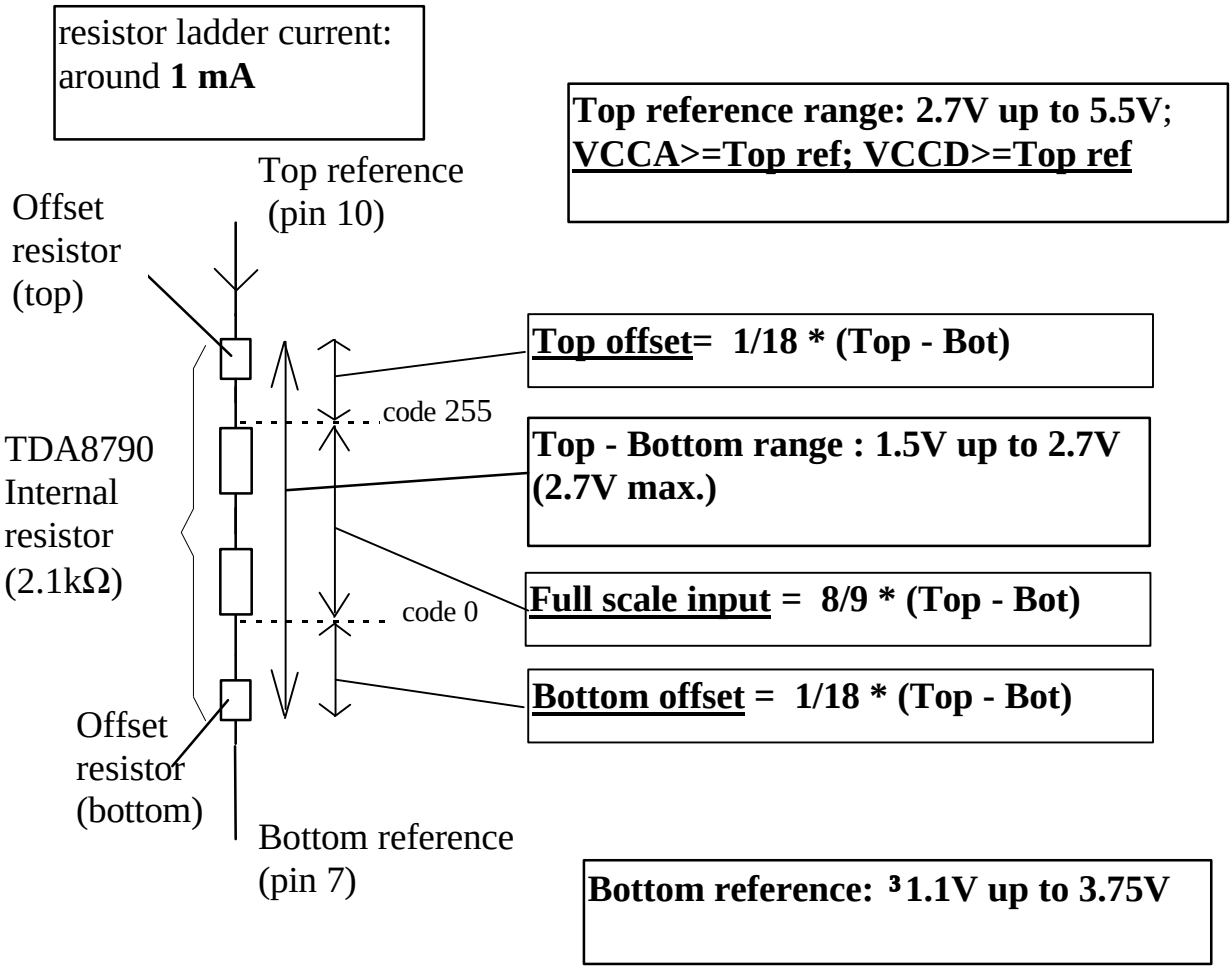
The full scale analog signal input range (FS) is given by:
FS=8/9 (Top ref. - Bottom ref.) ; The 8/9 coefficient is due to the two offset resistors.

The comparator voltage references are derived from a resistor ladder which is supplied through Vtop (pin 10) and Vbottom (pin 7). Therefore if the Vtop and Vbottom are not well regulated the A to D conversion will be affected.

Top reference (pin 10) is the highest voltage reference and the bottom reference (pin 7) is the lowest voltage reference. Consequently a current I is flowing from pin 10 to pin 7.

The typical value for the internal resistor ladder is 2.1kΩ at 25°C.

As shown in the following schematic the TDA8790M is versatile in the choice of the top voltage reference, bottom voltage reference and power supplies. So it will be easy to find top and bottom voltage references which fit with the majority of the applications.

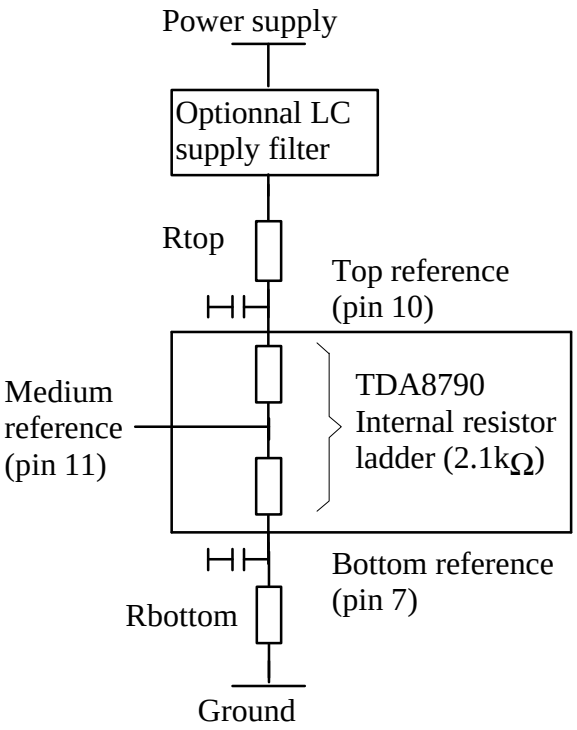


Regulation of Vtop & Vbottom depends on the level of cost and quality that are required by the customer application.

Several methods providing these voltage references are shown in this section.

5.1 TOP AND BOTTOM REFERENCES DERIVED FROM A POWER SUPPLY

If the power supply is well regulated a simple resistor string stucture will be efficient (see following figure).



It is possible that the top reference equal the power supply voltage. In that case the Rtop resistor can be removed. An optional filter can be added on the analog supply (depending on supply noise level).

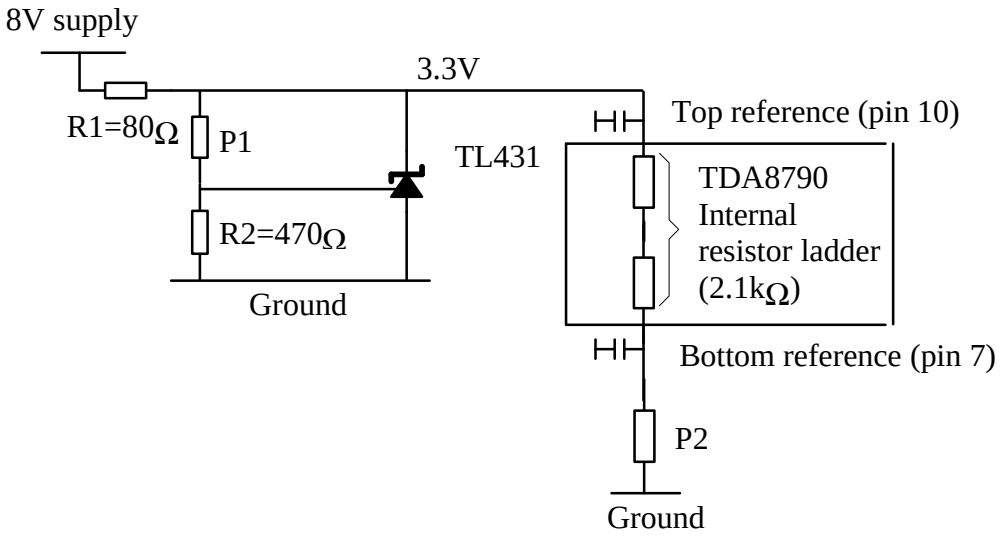
Typical voltages for a 3.3V application are 3.3V for the top reference and 1.2V for the bottom reference.
The current flowing through the 2.1kΩ resistor ladder is ≈1mA. So Rtop=0 and Rbottom=1.2 kΩ.
This is the solution implemented on the evaluation board.

Remarks: here, the spreads due to process and temperature are not taken into account.

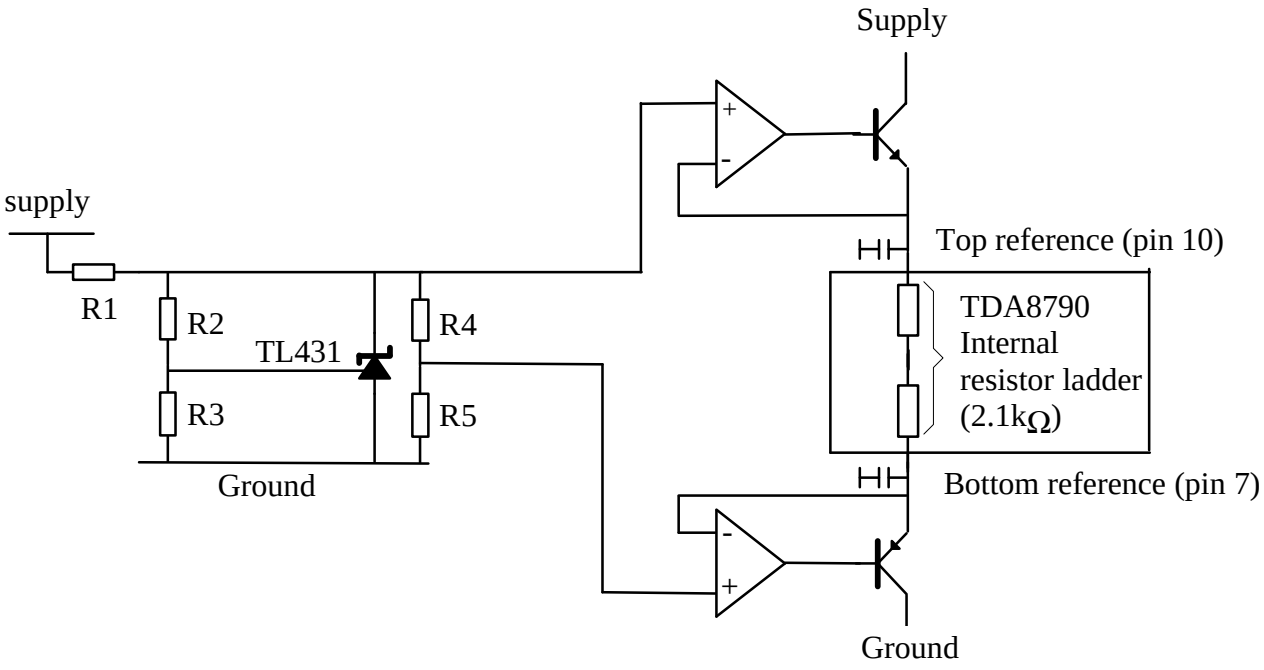
5.2 TOP AND BOTTOM REFERENCES DERIVED FROM REFERENCE VOLTAGE REGULATOR(S)

In some cases (noise on supply, several ADC's mounted in parallel ...) solutions with precision regulators (Philips uA723, Texas TL431,...) may be preferred.

TL431 output = 2.5 *(1+P1/R2) V



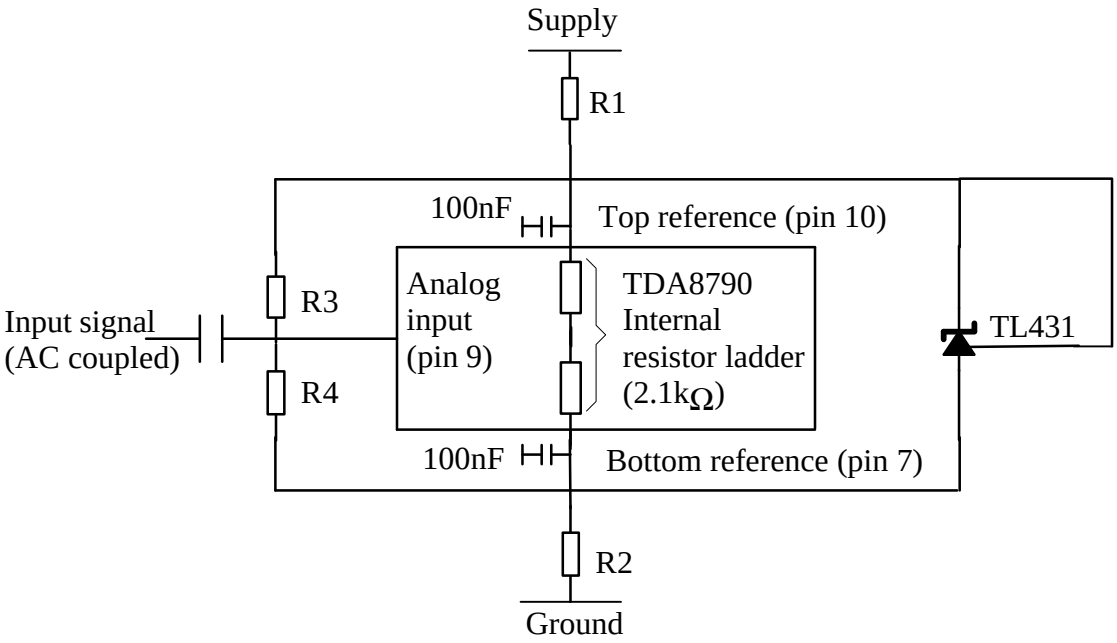
If several ADC are mounted in parallel, or if a very high precision of the voltage references over the whole temperature range is required, the following schematic can be used :



Operational amplifiers with a low input offset should be used. The transistor types depend on the number of TDA8790M mounted in parallel. (1 mA typ. for one TDA8790M)

If only one ADC is used the operational amplifier and the transistor which drive the top reference can be skipped. In this case, the voltage regulator directly drives the top reference.

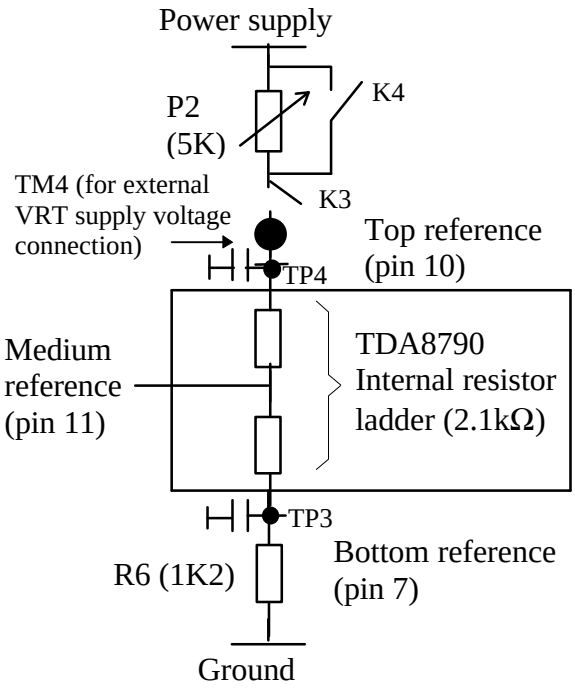
In the following electrical diagram, top and bottom references are regulated by only one component (TL431):



The (top - bottom) difference is set at 2.5V by the TL431, so the full scale input is set at 8/9*2.5=2.22V. In addition the input offset is set at (Vtop+Vbottom)/2 by two equal resistors (R3 and R4).
In this case the TL431 maintains the (top - bottom) difference at 2.5V over temperature and supply variations. Because the input offset is derived from the top and bottom references, it is also regulated at (Vtop+Vbottom)/2 over the temperature and supply variations.
Using this method it is possible to drive the input offset and the top and bottom references of several TDA8790M with a very good matching with only one TL431.
Typical resistor values for a 5V application and for one TDA8790M are:
R3=R4=2.2 kΩ, R1=R2=150 Ω. The current flowing trough the R1, R2 resistors is around 8 mA (The TL431 requires a minimum current to provide a good regulation).

5.3 ON-BOARD PRACTICAL REFERENCE VOLTAGES GENERATION

Pins VRT and VRB are decoupled to ground by 22nF ceramic capacitors.



VRT is derived from VDD through potentiometer P2 = 5 kΩ. It is also possible to force VRT to VDD using switch K4 to short-circuit potentiometer P2 :
Normally when VDD is set at +3.3V it is possible to short potentiometer P2 via switch K4 to set VRT to +3.3V = VDD.
When VDD=5V, potentiometer P2 is used to set VRT to a voltage different from VDD (for example, as initially set on the board, +3.3V).

Using K3 to disconnect potentiometer P2 from the A/D converter top reference input pin, it is possible to input the top reference voltage directly through grip point TM4 (and the associated ground TM5).

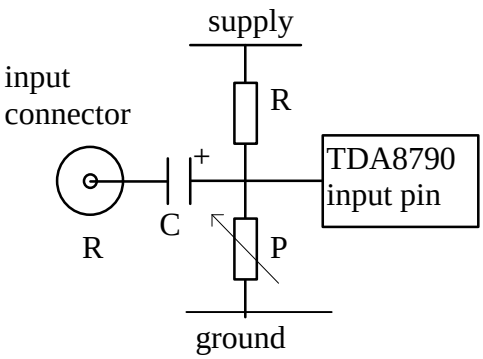
On the TDA8790M evaluation board, the VRB pin of the TDA8790M is connected to ground through a fixed 1.2 kΩ resistor (R6). The R6 resistor value has been chosen so that VRB be equal to +1.25V when VRT is equal to +3.3V.
Thus for this board, whichever the TDA8790M voltage supply, the recommanded VRT voltage is VRT = +3.3V when VDDA >= +3.3V, and VRT = VDDA when VDDA < +3.3V.
If necessary the R6 resistor can be replaced with another resistor of a different value for thorough evaluation of the A/D converter. However the VRB voltage should stay above +1.1V in any case.
Test points TP3 and TP4 allow to measure respectively VRB and VRT voltages.

6. INPUT OFFSET

When AC coupling is used with the TDA8790 it is necessary to provide an input offset in order to respect the TDA8790 full scale input range.
Relations between the Vtop reference, the Vbottom reference, the maximum amplitude of the analog signal and the input offset are:
Maximum amplitude of analog signal is (Vtop-Vbot)* 8/9 and the input signal is centered around the input offset which is (Vtop+Vbottom)/2.
Consequently, if Vtop = 3.3 V and if Vbottom = 1.2 V the maximum amplitude of the analog signal is 1.8 V and the input offset is 2.25V; code 0 is obtained for a 1.316V input, and code 255 is obtained for a 3.184 V input.

Input offset can be provided by many different methods; several methods are explained in this section.

6.1 INPUT OFFSET DERIVED FROM A RESISTOR BRIDGE



When a resistor bridge is used to provide an offset the current flowing through the resistors must be at least 10 times greater than the signal current (TDA8790 analog input current is 0 to 9µA) in order to guarantee the stability of the input offset. Consequently the resistive value of this resistor string must be below 30 kΩ (with a 3 V supply).

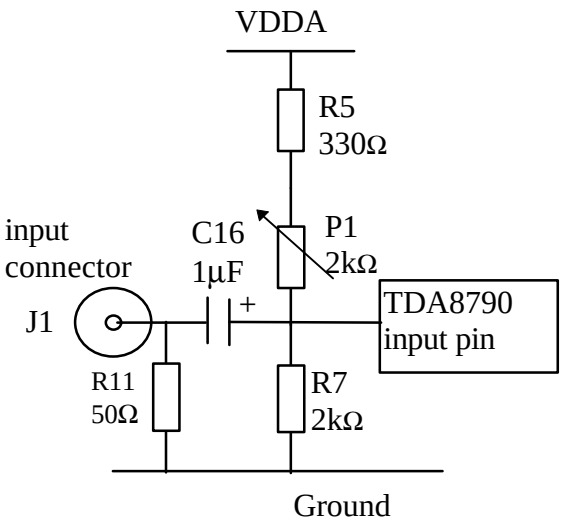
If the input signal generator used to test the TDA8790 requires a 50 Ω load, R must be set at 73.33 Ω and P at 157.14 Ω (Vtop=supplies=3.3 V,Vbottom=1.2 V), in order that the dynamic impedance (R & P in parallel) be 50 Ω.

Remarks:

- This method provides a correct input offset but the current flowing through the resistor bridge is high: 14mA (R=75Ω, P=157Ω and 3.3V supply).

6.2 INPUT OFFSET PRACTICAL GENERATION ON BOARD

In order to reduce this current consumption another method is used on board but it requires at least one more component (one resistor) :
The analog signal input offset is derived from the ADC analog supply through a resistor bridge (R1, R7 and potentiometer P1). It is adjustable thanks to P1.



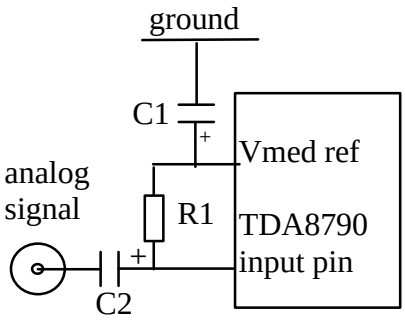
R11 is equal to the output load of the external signal generator. C16 allows ground connection between R2 and (R5+ P1)//R7 in dynamic mode. Typical values when a 50 Ω signal generator is used are: R11=50 Ω, R5=330 Ω, R7=2 kΩ P1=2 kΩ (set approximately to 1.7 kΩ) , then the current flowing through the resistor bridge is only 750 µA with a 3.3 V VDD.

- When it is possible, it is better to replace the potentiometers by fixed resistors. This will avoid possible distortion effects on the input signal due to the capacitive components of the potentiometers.

- It can be difficult to obtain the exact output load and the exact input offset when they are made up of fixed resistors, because the accuracy of the resistors is limited. Consequently in some professional applications it is better to provide the correct load and the correct input offset by means of operational amplifiers.

6.3 INPUT OFFSET DERIVED FROM THE MEDIUM REFERENCE

In this case the input pin is connected to the medium voltage reference (pin 8) by the means of a resistor (R1). The medium voltage reference must be well decoupled by a capacitor (C1). The input impedance of the AD converter is given by R1 in parallel with Zin.

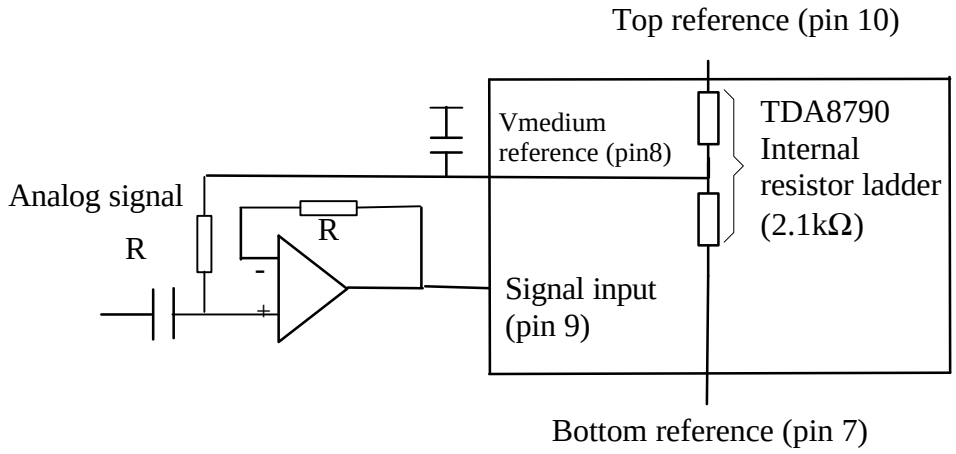


This method gives good results in the following domains : high common mode supply rejection (because both the voltage references and the input offset are derived from the same supply), very low noise level and low cost.
R1*C1 product must be high enough in order to avoid a coupling between the input signal and the medium reference.
(C1=4.7µF for example)
The offset on the input pin is:
Vmed - (4.5µA*R1)

6.4 INPUT OFFSET PROVIDED BY AN OPERATIONAL AMPLIFIER

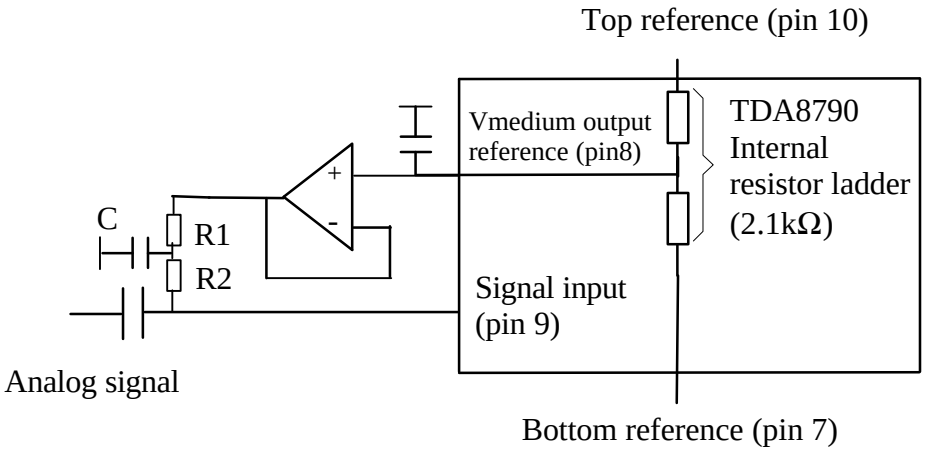
The middle output reference voltage and a low input offset operational amplifier can be used to provide an accurate input offset. Several methods can be used :

1°)



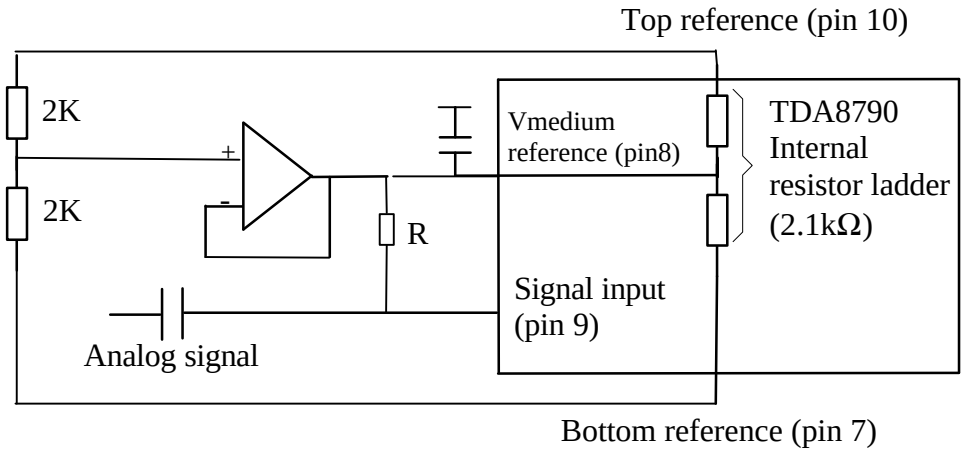
The R resistor in the op-amp loop compensates the offset due to the R resistor connected to Vmed. (R=1kΩ; C=1µF).

2°)



The amplifier does not need a high bandwidth, but the time necessary to load the C capacitor at ‘power on’ depends on.the op.amp maximum output current. The input impedance is R2 // Zin. Zin is the A/D converter input impedance.

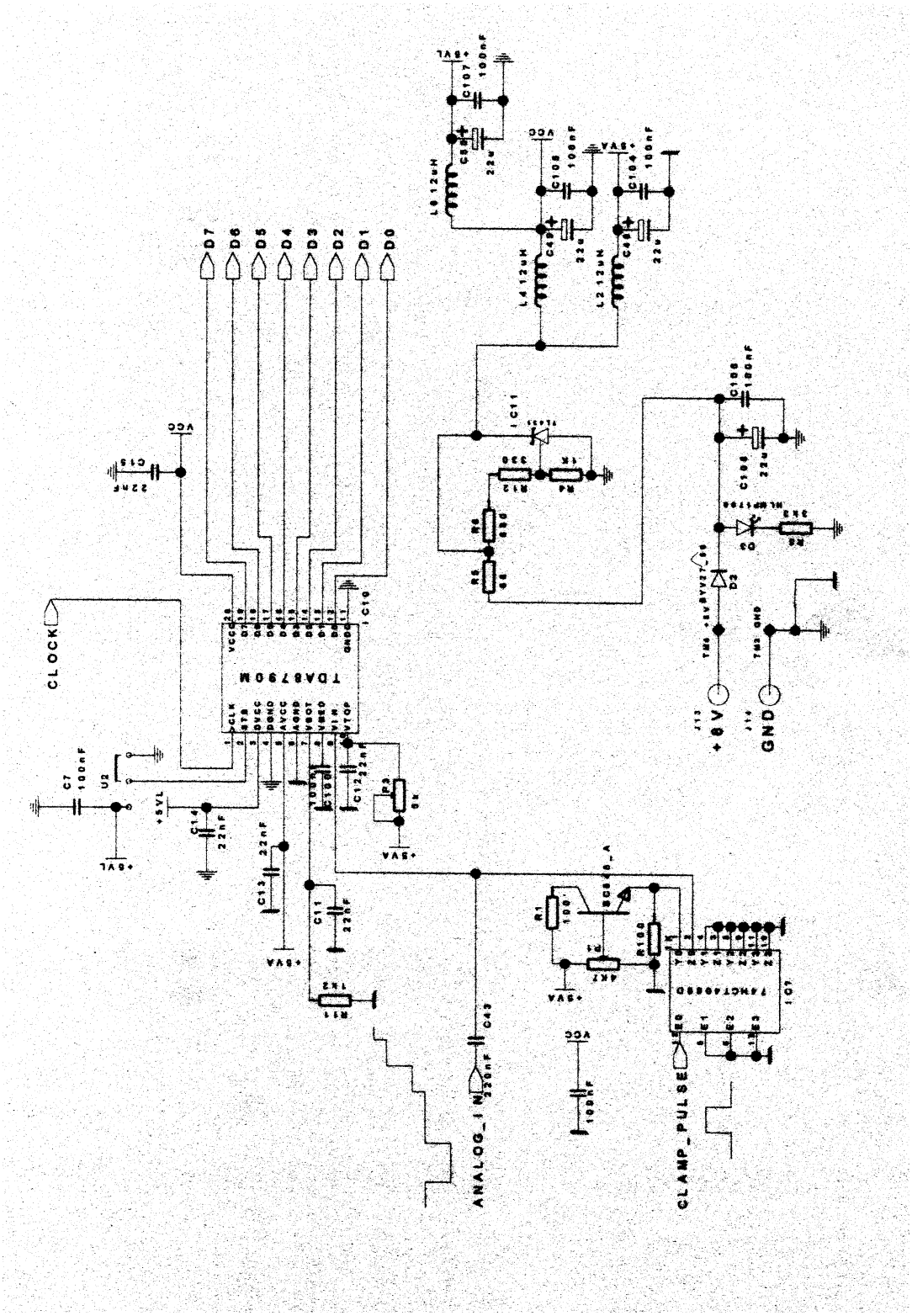
3°)



Medium reference is derived from top and bottom reference (input impedance is R // Zin).

7. CLAMP FOR VIDEO SIGNALS

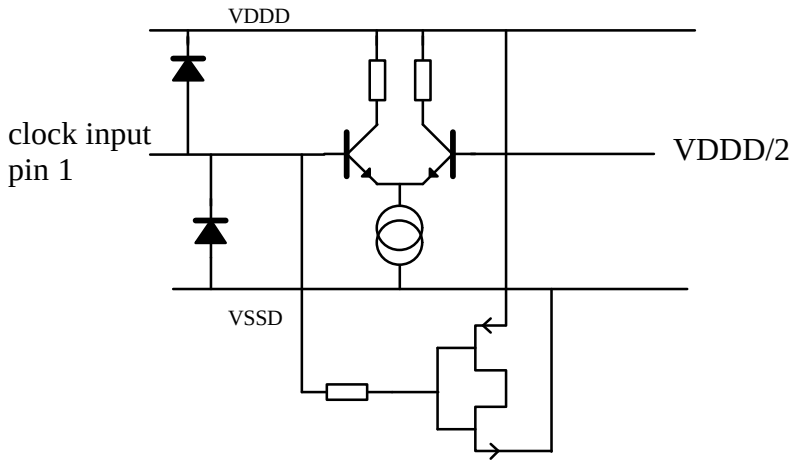
In case the TDA8790M is used for video signals digitization, a clamp circuit can prove useful. The following schematics shows the principle of such a clamp circuit (temperature variations are NOT compensated).


D7
D6
D5
D4
D3
D2
D1
D0
VCC
CLOCK
TDA8790M
+8V
GND
ANALOG_IN
CLAMP_PULSE
74HCT4066D

8. CLOCK

8.1 CLOCK INPUT

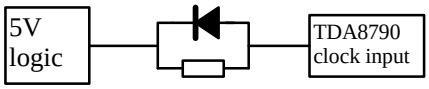
On the demo-board several methods can be used (depending on switch positions) to provide the ADC clock (see sections 2,3). Precautions must be taken if the high clock level is higher than the VDDD level.
In fact, the TDA8790 clock input (pin 1) is protected by diodes (see figure) :



If the high clock level is greater than VDDD+0.5 V, a current will flow between the clock input & VDDD through the protection diode. This will affect the proper operation of the A/D converter.
Consequently, it is necessary to keep the high clock level below VDDD+0.5 V.
Several methods can be used to limit high clock level :

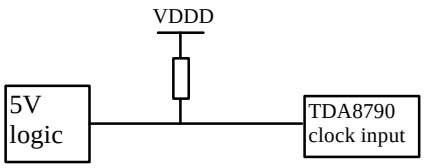
1- Use of a 3 V logic device as a 5 to 3 V interface (Philips LVC logic family for example).

2- Use of a parallel resistor/diode network in series with 5 V output (solution used on the evaluation board).

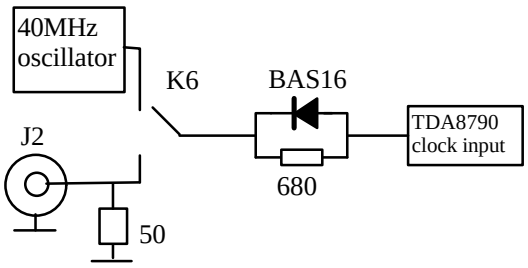


The resistor limits current and voltage supplied to the TDA8790. The diode allows a faster high to low transition (R=350Ω, D=BAS16/BAS32...).

3- In case of 5 V logic with an open drain output, use a pull-up resistor connected to the low voltage supply.



8.2 ACTUAL IMPLEMENTATION ON THE EVALUATION BOARD



The resistor limits current and voltage supplied to the TDA8790. The diode allows a faster high to low transition (R=680Ω, D=BAS16/BAS32...).

Using switch K6 it is possible to choose between external (plug J2) and on-board (40 MHz oscillator, Q1) clock for the A/D converter TDA8790M.

8.3 CLOCK JITTER

If the clock jitter and the slope of the analog input signal are high, sampling errors can appear.

Example :

The equation of a sinewave signal is **s(t)=A/2 sin(2 p F t)**, where **A** is the ADC full scale amplitude (**A=255 LSB**) and **F** is the sinewave frequency.
The slope of this signal is given by: **ds(t)/dt=A/2 2 p F cos(2 p F t)**
This slope is maximum when t=0 (input voltage level is around middle code 127/128):
ds(0)/dt=A p F Volt/second.
That means that the middle code is available at the ADC input only during:
Tlsb=LSB/(A p F)=(255 p F)$^{-1}$ second.
If the full scale sinewave frequency is **F = 10 MHz**, then **Tlsb = 124 ps**
Consequently the clock jitter must be lower than this value.
If a 20 MHz full scale sinewave is being sampled the jitter must be lower than 62 ps.

Remarks:
If the sample clock frequency and the input signal frequency have the same jitter (or phase noise), the sampling error due to jitter can be avoided. Therefore it is not suitable to do precise dynamic measurements of the ADC characteristics with the on board quartz oscillator. (Except if the input signal frequency and the quartz oscillator frequency are correlated).

9. 8 BIT D/A CONVERTER

An 8 bit 5 V supply/TTL input DAC TDA8702 (IC2) allows rough A/D converter evaluation with a scope or a spectrum analyzer. Analog output level is in the range of 3.6 to 5 V (with a high impedance load).

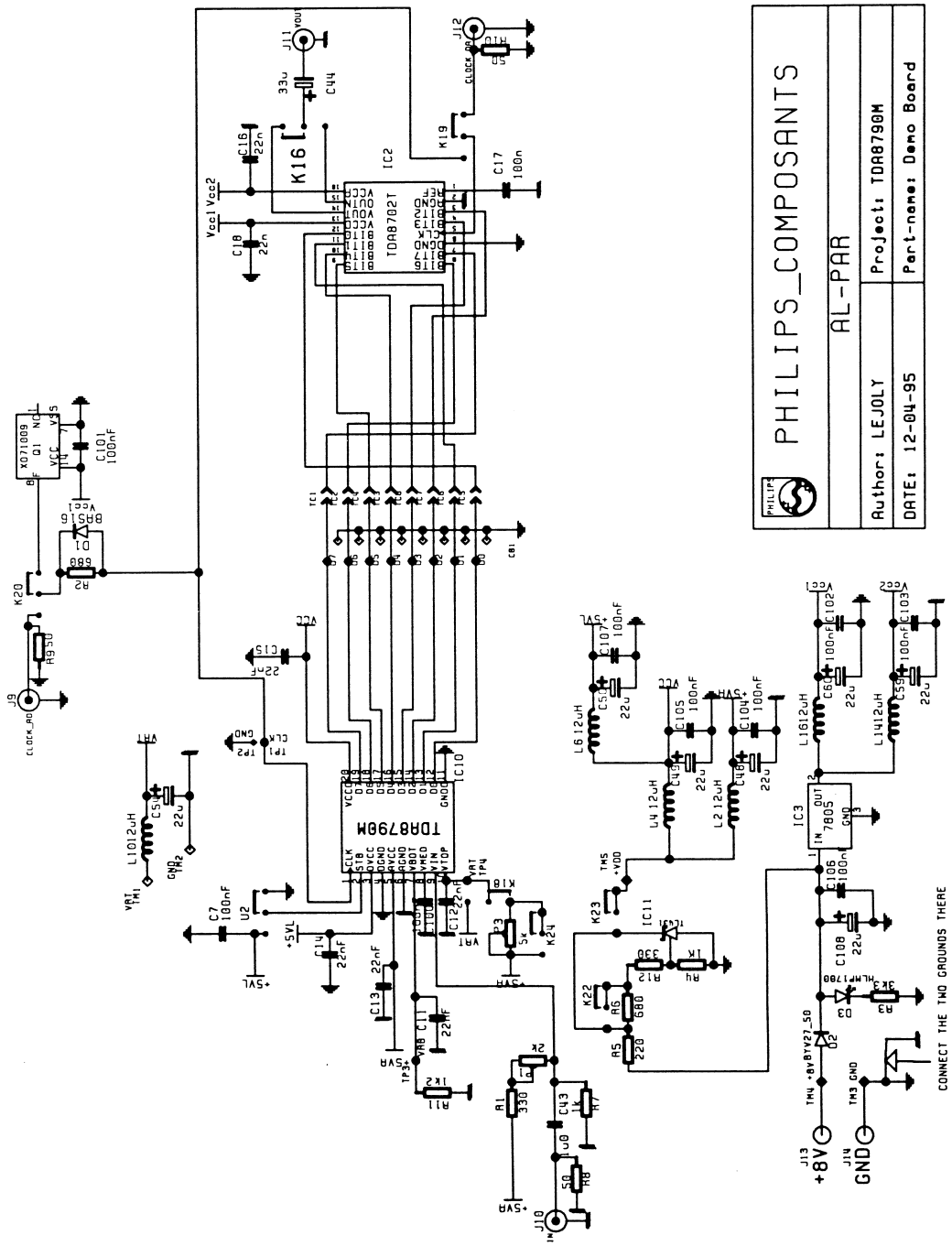
It is possible to switch the reconstructed Voutput signal present on plug J4 between non inverted and inverted via switch K8.
The D/A converter supplies are set to 5 V (by means of a 7805 regulator, IC4).

The D/A converter clock can be chosen, via switch K7, between A/D converter clock (selected between on-board and external via switch K6) and external clock (input via plug J3).

10. DEMO BOARD DOCUMENTATION : ELECTRICAL DIAGRAM, COMPONENT LIST & COMPONENTS IMPLANTATION

10.1 ELECTRICAL DIAGRAM

(see next page)


PHILIPS_COMPOSANTS
AL-PAR
Author: LEJOLY
DATE: 12-04-95
Project: TDA8790M
Part-name: Demo Board
TDA8790M
TDA8702T
CONNECT THE TWO GROUNDS THERE

10.2 COMPONENT LIST

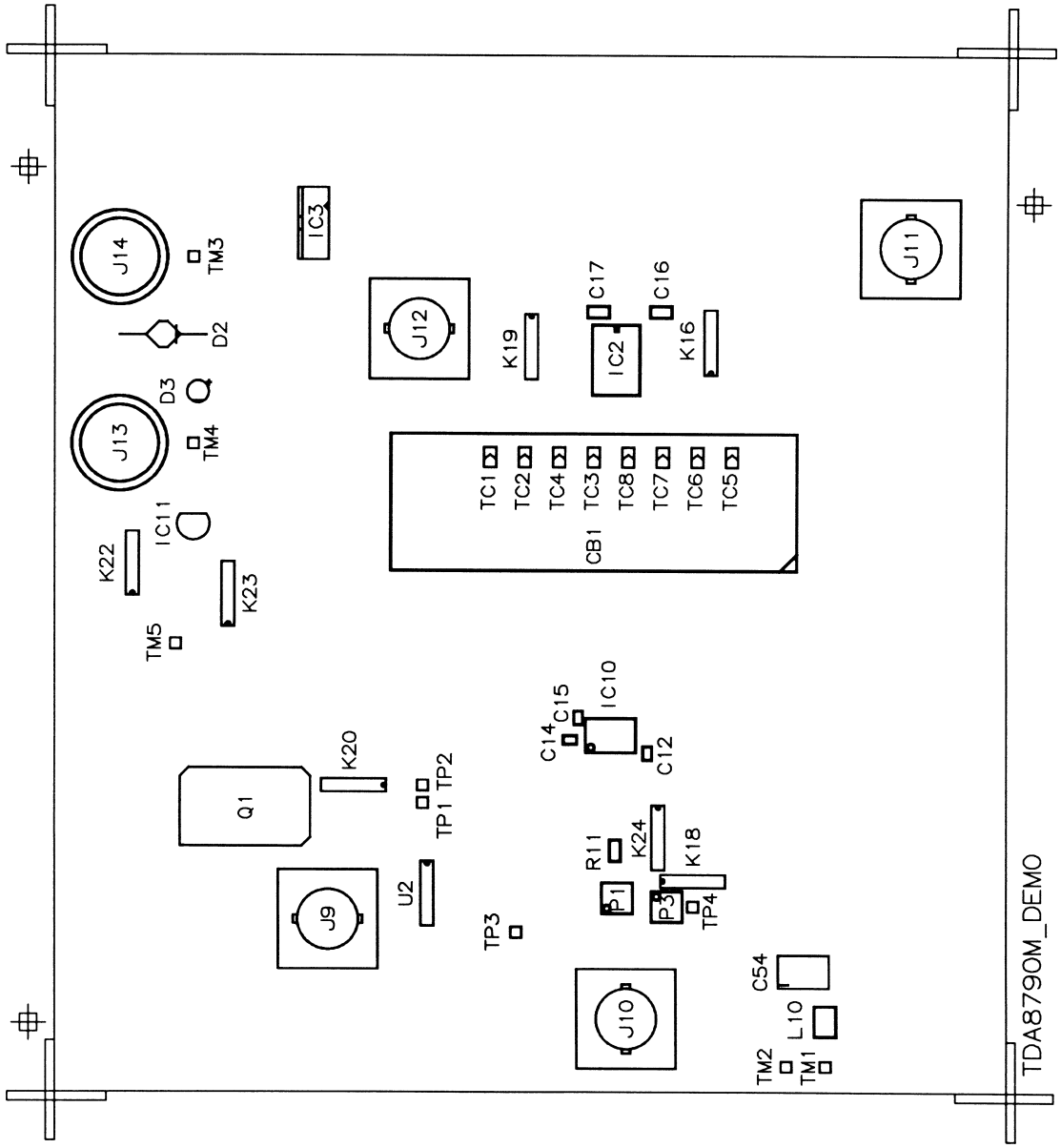
Reference	Value	Component
B1		BANANA PLUG (+8V)
B2		BANANA PLUG (GROUND)
C1	100nF	C1206
C2	22 µF	SPRAGUE_293D_D
C3	22 µF	SPRAGUE_293D_D
C4	22 µF	SPRAGUE_293D_D
C5	100 nF	C1206
C6	100 nF	C1206
C7	100 nF	C1206
C8	22 nF	C805
C9	22 nF	C805
C10	22 nF	C805
C11	22 nF	C805
C12	22 nF	C1206
C13	100 nF	C805
C14	100 nF	C1206
C15	100 nF	C1206
C16	1 µF	C1812
C17	22 µF	SPRAGUE_293D_D
C18	22 µF	SPRAGUE_293D_D
C19	22 µF	SPRAGUE_293D_D
C20	100 nF	C1206
C21	100 nF	C1206
C22	100 nF	C1206
C23	22 nF	C1206
C24	22 nF	C1206
C25	33 µF	SPRAGUE_293D_D
C26	22 µF	SPRAGUE_293D_D
CB1		8 BITS CONNECTOR
D1		BAS16
D2		BYV27_50
D3		HLMP1700 (GREEN)
IC1		TDA8790M

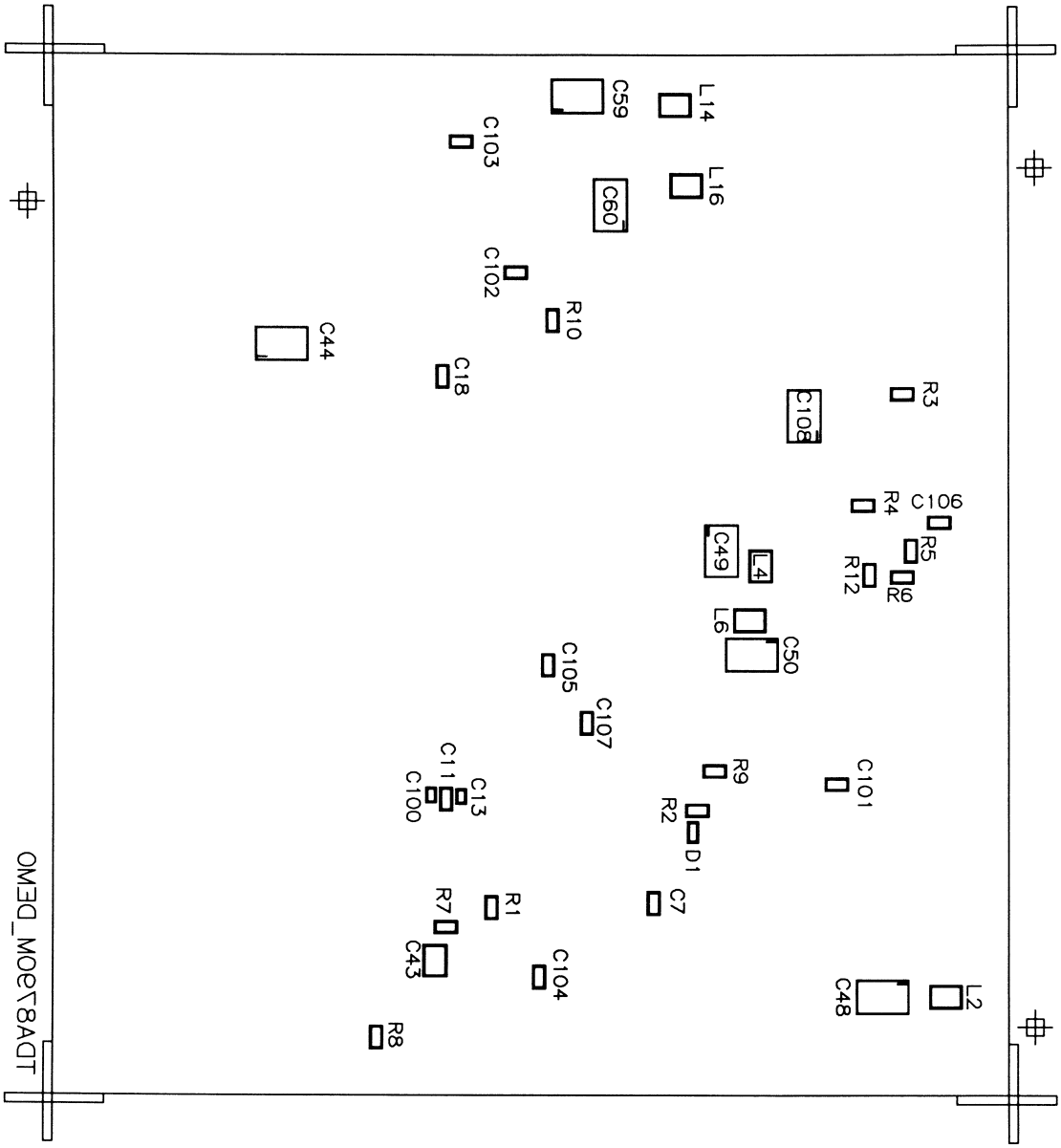
IC2		TDA8702T
Reference	**Value**	**Component**
IC3		TL431
IC4		7805
J1		BNC
J2		BNC
J3		BNC
J4		BNC
K1		SWITCH
K2		SWITCH
K3		SWITCH
K4		SWITCH
K5		SWITCH
K6		SWITCH
K7		SWITCH
K8		SWITCH
L1	12µH	LQH4N
L2	12µH	LQH4N
L3	12µH	LQH4N
L4	12µH	LQH4N
L5	12µH	LQH4N
L6	12µH	LQH4N
P1	2K	3224W
P2	5K	3224W
Q1	40MHz	X071009
R1	100	RC01
R2	680	RC01
R3	330	RC01
R4	1K	RC01
R5	330	RC01
R6	1K2	RC01
R7	1K	RC01
R8	680	RC01
R9	50	RC01
R10	50	RC01
R11	50	RC01
TC1-TC8		SOLDER POINTS
TM1		GRIP POINT (+8V)

TM2		GRIP POINT (GROUND)
TM3		GRIP POINT (A/D converter VDD)
Reference	**Value**	**Component**
TM4		GRIP POINT (A/D converter top ref.)
TM5		GRIP POINT (GROUND)
TP1-TP2		TEST POINTS (A/D converter clock)
TP3		TEST POINT (A/D converter bottom reference)
TP4	J14	TEST POINTS (A/D converter top reference)

10.3 COMPONENTS IMPLANTATION

(See next page)


J14
TM3
IC3
J12
K19
C17
C16
J11
D2
IC2
K16
D3
J13
TM4
TC1
TC2
TC4
TC3
TC8
TC7
TC6
TC5
CB1
IC11
K22
K23
TM5
C14
C15
IC10
C12
K20
Q1
TP1
TP2
R11
K24
K18
U2
J9
P1
P3
TP4
TP3
C54
J10
L10
TM2
TM1
TDA8790M_DEMO


C59
L14
C103
L16
C60
C102
R10
C44
C18
R3
C108
C106
R4
R5
C49
L4
R12
R6
L6
C50
C105
C107
C11
C13
C100
R9
C101
R2
D1
R7
R1
C7
C43
C104
C48
L2
R8
TDA8790M_DEMO